This listing of claims will replace all prior versions,
and listings, of claims in the application:

Claims 1-49 (canceled)

1   Claim 50 (new): An apparatus for performing parity check
2   message passing decoding operations, the apparatus
3   comprising:
4   a message source for supplying at least one set
5   of Z K-bit messages from any of at least L sets of Z K-
6   bit messages, where Z is a positive integer greater than
7   one and K and L are non-zero positive integers;
8   a node processor including a plurality of node
9   processing units, each node processing unit for
10   performing at least one of a parity check constraint node
11   processing operation and a parity check variable node
12   processing operation; and
13   a switching device coupled to the message
14   source and to the node processing unit, the switching
15   device for passing sets of Z K-bit messages between said
16   message source and said node processor and for
17   re-ordering the messages in at least one of said passed
18   sets of messages in response to switch control
19   information.

1   Claim 51 (new): The apparatus of claim 50,
2   wherein said message source is a memory device;
3   and
4   wherein each of said plurality of node
5   processing units is a variable node processing unit.

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1 Claim 52 (new): The apparatus of claim 50, further
2 comprising:
3   a message ordering control module coupled to
4 said switching device for generating said switch control
5 information used to control the reordering of messages in
6 said at least one set of messages.

1 Claim 53 (new): The apparatus of claim 52, wherein the
2 switching device includes circuitry for performing a
3 message rotation operation to reorder messages included
4 in a set of messages.

1 Claim 54 (new): The apparatus of claim 52, wherein the
2 message ordering control module stores information on the
3 order sets of messages are to be received from said
4 message source and information indicating what reordering
5 of messages is to be performed by said switch on
6 individual sets of messages received from said message
7 source.

1 Claim 55 (new): The apparatus of claim 52, wherein the
2 message ordering control module is further coupled to
3 said message source and sequentially generates set
4 identifiers, each set identifier controlling the message
5 source to output a set of messages.

1 Claim 56 (new): The apparatus of claim 55, wherein each
2 set identifier includes a single memory address.

4

1   Claim 57 (new): The apparatus of claim 52, wherein said
2   plurality of node processing units includes Z node
3   processing units arranged in parallel, each one of the Z
4   node processing units operating in parallel to process a
5   different message in each set of Z messages passed
6   between said message source and said node processor.

1   Claim 58 (new): The apparatus of claim 57, wherein said
2   message source includes an identifier input which allows
3   each set of messages to be addressed as a unit.

1   Claim 59 (new): The apparatus of claim 57, wherein each
2   of said plurality of node processing units performs a
3   variable node processing operation.

1   Claim 60 (new): The apparatus of claim 57,
2   wherein the decoder control device is further
3   coupled to said message ordering control module.

1   Claim 61 (new): The apparatus of claim 52, further
2   comprising a decoder control module coupled to the
3   message ordering module, the decoder control module
4   including means for supplying information to the message
5   ordering module used to control the order in which each
6   of the L sets of Z messages are output by said message
7   source.

1   Claim 62 (new): The apparatus of claim 61, further
2   comprising a degree memory coupled to the node processor
3   for storing a set of node degree information.

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1   Claim 63 (new): The apparatus of claim 62, wherein the

2   control device further generates a node index used to

3   determine which node degree information in the stored set

4   of node degree information is to be supplied to the node

5   processor at any given time.

1   Claim 64 (new): The apparatus of claim 50, further

2   comprising:

3   a second node processor coupled to said message source,

4   the second node processor including a second plurality of

5   node processing units, each of the second plurality of

6   node processing units for performing constraint node

7   processing operation.

1   Claim 65 (new): The apparatus of claim 64, further

2   comprising:

3   a parity check verifier, coupled to said first

4   node processor, for determining from an output of each of

5   the first plurality of processing units included therein,

6   when a parity check decoding operation has been

7   successfully completed.

1   Claim 66 (new): A method of performing parity check

2   message passing decoding processing comprising the steps

3   of:

4   maintaining L sets of k-bit messages in a

5   message storage device, each set of K-bit messages

6   including first through Z messages, where L and Z are

7   positive integers greater than one and K is a non-zero

8   positive integer;

9   outputting one of said sets of K-bit messages

10   from the message storage device;

11   performing a message reordering operation on

12   said read set of K-bit messages to produce a reordered

13   set of Z K-bit messages; and

14   supplying, in parallel, the Z messages in the

15   reordered set of messages to a vector processor; and

16   operating the vector processor to perform parity check

17   message passing decoder operations using the Z supplied

18   messages as input.

1   Claim 67 (new): The method of claim 66, further

2   comprising: generating a message set

3   identifier indicating the set of Z messages to be output

4   by the message storage device.

1   Claim 68 (new): The method of claim 67, wherein the step

2   of   outputting one of said sets of K-bit

3   messages includes: performing a SIMD output operation

4   using said message set identifier to identify the set of

5   messages to be output.

1   Claim 69 (new): The method of claim 66, further

2   comprising: performing a second message

3   reordering operation, the second message reordering

4   operation being performed on the generated set of Z

5   decoder messages to produce a reordered set of generated

6   decoder messages.

1   Claim 70 (new): The method of claim 69, wherein the step

2   of performing a second message reordering operation

3   includes performing the inverse of the message reordering

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4   operation performed on said set of K-bit messages output

5   by the message storage device.

1   Claim 71 (new): The method of claim 70, wherein said

2   message reordering operation is performed as a function

3   of message set permutation information that includes

4   cyclic rotation information.

1   Claim 72 (new): The method of claim 66, further

2   comprising:

3   accessing stored message set permutation

4   information; and

5   wherein the step of performing a message

6   reordering operation includes the step of:

7   performing said reordering as a function of the

8   accessed stored message set permutation information.

1   Claim 73 (new): The method of claim 66,

2   wherein said parity check message passing

3   decoder operations are variable node low density parity

4   check processing operations, each variable node

5   processing operation including generating a decision

6   value, and

7   wherein the method further comprises:

8   examining decision values generated by

9   operating the vector processor to determine if a decoding

10   condition has been satisfied.

1   Claim 74 (new): A method of performing parity check

2   message passing decoding processing, the method

3   comprising the steps of:

4   operating a variable node vector processor to

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5 generate a set of Z K-bit messages, where Z is a positive

6 integer greater than one and K is a non-zero positive

7 integer; and

8   performing a message reordering operation on

9 the generated set of Z K-bit messages to produce a

10 reordered set of Z K-bit messages.

1 Claim 75 (new): The method of claim 74, wherein the step

2 of operating the node vector processor to generate a set

3 of Z K-bit messages, includes the step of:

4   performing, in parallel, Z node processing

5 operations, each node processing operation generating one

6 message in said set of Z K-bit messages.

1 Claim 76 (new): The method of claim 75, wherein

2 performing a message reordering operation on the

3 generated set of Z K-bit messages includes:

4   rotating the messages in the set of Z K-bit

5 messages by performing a switching operation to reorder

6 the messages in the set of messages.

1 Claim 77 (new): A method of performing parity check

2 decoder operations, the method comprising:

3   performing a message output operation to output

4 a set of messages;

5   performing a message reordering operation on

6 the output set of messages to produce a reordered set of

7 messages;

8   supplying the reordered set of messages to a

9 node processor including a plurality of variable node

10 processing units arranged in parallel; and

11   operating the plurality of variable node

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